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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/819,053	05/20/2000	Frank W. Ahern	101950-00027	9991

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EXAMINER	
AUVE, GLENN ALLEN	
ART UNIT	**PAPER NUMBER**
2111	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/819,053	AHERN, FRANK W.	
	Examiner	Art Unit	
	Glenn A. Auve	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7,8 and 24-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7,8 and 24-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Terminal Disclaimer

1. The terminal disclaimer filed on 25 April 2005 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of U.S. Pat. No. 6,070,214 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 25-30, 35, 40 and 44 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 25-30 are each rejected based on lack of positive antecedent basis of "The bridge" on line 1.

Claim 35 is rejected based on lack of positive antecedent basis of "those addresses appearing on said first bus" on line 2.

Claim 40 is rejected based on lack of positive antecedent basis of "said secondary interface" on lines 1-2.

Claim 44 is rejected because it is not clear how the second application specific integrated circuit can be said to comprise a plurality of ports coupled to said second interface for providing input/output when the second interface comprises the second application specific integrated circuit. Likewise it is not clear if applicant means to say that the first application specific integrated circuit comprises a plurality of ports coupled to said second interface for providing input/output.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1,2,4,5,7, and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Hong (as previously applied).

As to claims 1, 2, 4, 5, 7, and 8, Hong discloses a system for enabling device communication in an expanded computing device comprising a primary bus (note Figure 2, bus 158) coupled to a first IC (note Figure 2, local serial bridge 104) having a first register and a second register (i.e., wherein registers or buffers coupled at both ends of the redundant, unidirectional serial links 108 and 110 going in the direction from the local serial bridge to the remote serial bridge, with at least one register coupled at each end of each unidirectional link, are inherent to allow unidirectional data transfer along the links from the local serial bridge to the remote serial bridge), a secondary bus (note Figure 2, bus 160) physically remote from the primary bus coupled to a second IC (note Figure 2, remote serial bridge 114) having a third register and a fourth register (i.e., wherein registers or buffers coupled at both ends of the redundant, unidirectional serial links 108 and 110 going in the direction from the remote serial bridge to the local serial bridge, with at least one register coupled at each end of each unidirectional link, are inherent to allow unidirectional data transfer along the links from the remote serial bridge to the local serial bridge), a first serial link (note Figure 2, unidirectional links from local serial bridge to remote serial bridge) coupled between the first register and the third register, a second serial link (note Figure 2, unidirectional links from remote serial bridge to

local serial bridge) coupled between the second register and the fourth register, wherein the first IC is configured to enable the transfer of data to the second IC without using caching (i.e., wherein since the specification is silent as to the use of caching during data transfer long the serial links between the local serial bridge and the remote serial bridge, it meets the limitations of transferring data without using caching), wherein the first IC is an ASIC (note column 3, lines 2-15), wherein the second IC is adapted to transfer data to the first IC without using caching (i.e., wherein since the specification is silent as to the use of caching during data transfer long the serial links between the local serial bridge and the remote serial bridge, it meets the limitations of transferring data without using caching), and also discloses an interface (note Figure 1, elements 107,104,114) comprising an interface adapted to interface parallel data from a parallel data bus (Note Figure 2, bus 106) to a first bus (note Figure 2, bus 158) and a module (note Figure 2, local serial bridge 104) adapted to interface parallel data from the parallel data bus into serial data adapted to interface with a second remote bus (note Figure 2, bus 160), the module converting the parallel data to serial data without using caching, further comprising a first interface, the first interface configured to determine if a pending address provided thereto represents a transaction to be communicated to the second.

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 5,24-44,45-47 and 50-52 are rejected under 35 U.S.C. 102(e) as being anticipated by Conway et al., U.S. Pat. No. 6,425,033 B1 (previously cited).

As per claim 5, Conway shows an interface comprising an interface adapted to interface parallel data from a parallel data bus to a first bus; and a module adapted to interface the parallel data from the parallel data bus into serial data adapted to interface with a second remote bus, the module converting the parallel data to serial data without using caching (figs. 1A and 3). Conway shows all of the elements recited in claim 5.

As per claim 24, Conway shows An interface comprising a circuit adapter to couple a first bus having a parallel data bus (130), the circuit adapted to serially send the bus data over a link (104) to a physically remote second bus (140) without requiring or waiting for an incoming acknowledgement over the link before inaugurating a transfer of the serialized bus data over the link (in cols. 6-8 which describe how the system operates to transfer data between the two PCI buses over the serial link). Conway shows all of the limitations recited in claim 24.

As for claim 25, the argument for claim 24 applies. Conway also shows that the first bus is a PCI bus (abstract and fig.2). Conway shows all of the limitations recited in claim 25.

As for claim 26, the argument for claim 24 applies. Conway also shows that the circuit is an integrated circuit (inherent in modern electronic and computer components). Conway shows all of the limitations recited in claim 26.

As for claim 27, the argument for claim 26 applies. Conway also shows that the integrated circuit is an application specific integrated circuit (ASIC)(also inherent in modern electronic and computer components). Conway shows all of the limitations recited in claim 27.

As for claim 28, the argument for claim 24 applies. Conway also shows that the circuit is operable to exchange bus data according to a predetermined hierarchy giving the first bus a

higher level than the second bus (inherent in the PCI bridge, see at least PCI to PCI Bridge Architecture Specification section 5). Conway shows all of the limitations recited in claim 28.

As for claim 29, the argument for claim 24 applies. Conway also shows a first register adapted to hold parallel bus data (the buffers in figure 1A and also the queues in fig.3). Conway shows all of the limitations recited in claim 29.

As for claim 30, the argument for claim 29 applies. Conway also shows a second register adapted to hold received second bus data (the buffers in figure 1A and also the queues in fig.3). Conway shows all of the limitations recited in claim 30.

As per claim 31, Conway shows a bridge accessible by a processor for expanding access over a first bus to a second bus, said first bus and said second bus each being adapted to separately connect to respective ones of a plurality of bus-compatible devices, said bridge comprising: a link (104); a first interface coupled between said first bus and said link (fig.1A, the parallel/serial transceiver); and a second interface adapted to couple between said second bus and said link (fig.1A, the parallel/serial transceiver), said first interface and said second interface being operable to transfer bus data serially through said link without waiting for an incoming acknowledgment over said link before inaugurating a transfer of said bus information over said link (in cols. 6-8 which describe how the system operates to transfer data between the two PCI buses over the serial link). Conway shows all of the limitations recited in claim 31.

As for claim 32, the argument for claim 31 applies. Conway also shows that the first and second interfaces are operable to exchange bus data according to a predetermined hierarchy giving the first bus a higher level than the second bus (inherent in the PCI bridge, see at least PCI to PCI Bridge Architecture Specification section 5). Conway shows all of the limitations recited in claim 32.

As for claim 33, the argument for claim 31 applies. Conway also shows that said first bus and said second bus each have a plurality of signaling lines for enabling bus-compatible devices to negotiate bus communications, said first interface being operable in response to a pending transaction on said first bus to begin processing said pending transaction and to apply a retry signal to at least one of said signaling lines of said first bus before the pending transaction on said first bus has been transmitted to and acknowledged by said second bus (inherent in PCI bus operation). Conway shows all of the limitations recited in claim 33.

As for claim 34, the argument for claim 33 applies. Conway also shows that less than all of the information on the signaling lines of said first bus is transmitted by said first interface over said link (inherent in PCI bridge operation). Conway shows all of the limitations recited in claim 34.

As for claim 35, the argument for claim 31 applies. Conway also shows that said first interface is selectively responsive to those addresses appearing on said first bus that are on a predetermined schedule of addresses corresponding to the bus-compatible devices accessible through said second bus, in order to avoid responding to addresses corresponding to other ones of the bus-compatible devices on said first bus (inherent in the PCI bridge, which includes address registers and configuration as claimed, see at least PCI to PCI Bridge Architecture Specification section 6). Conway shows all of the limitations recited in claim 35.

As for claim 36, the argument for claim 35 applies. Conway also shows a register for storing the predetermined schedule (inherent in the PCI bridge, which includes base address registers as claimed, see at least PCI to PCI Bridge Architecture Specification section 6). Conway shows all of the limitations recited in claim 36.

As for claim 37, the argument for claim 35 applies. Conway also shows that said first interface comprises: a first register for storing said predetermined schedule, said second

interface comprising: a second register for storing said predetermined schedule (inherent in the PCI bridge, which includes base address registers as claimed, see at least PCI to PCI Bridge Architecture Specification section 6). Conway shows all of the limitations recited in claim 37.

As for claim 38, the argument for claim 36 applies. Conway also shows that said register is operable to establish with respect to said first bus a base address for one or more of the bus-compatible devices on said second bus (inherent in the PCI bridge, which includes base address registers as claimed, see at least PCI to PCI Bridge Architecture Specification section 6). Conway shows all of the limitations recited in claim 38.

As for claim 39, the argument for claim 31 applies. Conway also shows a register for establishing with respect to the first bus a base address for one or more of the bus compatible devices on the second bus (inherent in the PCI bridge, which includes base address registers as claimed, see at least PCI to PCI Bridge Architecture Specification section 6). Conway shows all of the limitations recited in claim 39.

As for claim 40, the argument for claim 31 applies. Conway also shows that the first interface and second interface are operable to permit communication between bus compatible devices on the second bus without routing through the first bus (inherent in the PCI bridge, wherein transactions that are only within the address range of devices on the second bus are not passed through the bridge, see PCI to PCI Bridge Architecture Specification section 6.1). Conway shows all of the limitations recited in claim 40.

As for claim 41, the argument for claim 31 applies. Conway also shows that said first interface and said second interface comprise: a first and a second programmable logic device connected between said link and said first bus and said second bus, respectively (fig.1A and 3 where there are packetizers and control circuits in the interfaces). Conway shows all of the limitations recited in claim 41.

As for claim 42, the argument for claim 31 applies. Conway also shows that said first interface and said second interface comprise: a first and a second application-specific integrated circuit connected between said link and said first bus and said second bus, respectively (fig.1A and 3 where there are packetizers and control circuits in the interfaces). Conway shows all of the limitations recited in claim 42.

As for claim 43, the argument for claim 42 applies. Conway also shows that said first and said second application-specific integrated circuit are identically structured and each have a control pin for receiving a control signal to establish operation in one of two modes (col.7, lines 35-47). Conway shows all of the limitations recited in claim 43.

As for claim 45, the argument for claim 31 applies. Conway also shows that said processor is interrupt-driven, said second interface being operable to transmit through said link to said first interface interrupt signals destined to interrupt the processor (inherent in PCI operation, see PCI to PCI Bridge Architecture Specification section 11). Conway shows all of the limitations recited in claim 45.

As for claim 46, the argument for claim 45 applies. Conway also shows that said processor is responsive to error signals, said second interface being operable to transmit through said link to said first interface error signals destined to affect the processor (inherent in PCI operation, see PCI to PCI Bridge Architecture Specification section 8). Conway shows all of the limitations recited in claim 46.

As for claim 47, the argument for claim 31 applies. Conway also shows that said first bus operates at a predetermined clock speed, said link being operable to propagate data between said first interface and said second interface at a bit transfer rate greater than said predetermined clock speed (inherent in that the serial link is described as operating at Gigabaud

rate while the PCI bus operates at a lower speed). Conway shows all of the limitations recited in claim 47.

As for claim 50, the argument for claim 31 applies. Conway also shows that the second bus is a PCI bus (at least in the abstract and col.2). Conway shows all of the limitations recited in claim 50.

As for claim 51, the argument for claim 31 applies. Conway also shows that said second interface is operable in response to a transaction from said link signifying an initial read request, to fetch and pre-fetch data from a competent one of the bus-compatible devices on said second bus for transmission back over said link in order to satisfy pending and anticipated transactions (fig.3 which includes various queues for storing data to be transmitted via the serial link to the other interface circuit). Conway shows all of the limitations recited in claim 51.

As for claim 52, the argument for claim 31 applies. Conway also shows that said first interface and said second interface are operable to permit at least one of the bus-compatible devices on said second bus to address one or more of the bus-compatible devices on said first bus using on said second bus substantially the same type of addressing as is used to access devices on said second bus (abstract and col.2, wherein both of the buses are PCI buses and the system is arranged such that devices one either bus can access the other bus). Conway shows all of the limitations recited in claim 51.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having

ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hong, 5,764,924 in view of Drottar et al., 6,333,929 (hereinafter Drottar).

Hong fails to disclose that the first interface is adapted to send a tag to the second interface indicative of a bus transaction type.

Drottar discloses that a first bridge is adapted to send a tag (i.e., opcode) to a second bridge indicative of a bus transaction type (note abstract, column 2, lines 13-33, column 3, lines 6-17, column 14, line 22 – column 15, line 34).

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the use of a tag to send transaction type information from the first interface of Hong to the second interface of Hong, as Drottar teaches, so as to allow a distributed arrangement of host computers and I/O systems, providing the convenience of remote I/O access while maintaining compatibility with current commands, drivers, devices, and standards, as Drottar teaches in column 2, line 54 – column 3, line 5.

10. Claims 48 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Conway in view of Hong.

As for claim 48, the argument above for claim 47 applies. Conway shows a gigbit serial link (at least in fig.3) but does not specifically show that the link comprises a pair of simplex links for sending information in opposite directions. Hong shows a PCI to PCI link system with a serial link comprising a pair of unidirectional links that operate at one gigabit per second to send information in opposite directions (col. 3, lines 28-32 and fig.2, (108 or 110)). It would have been obvious to one of ordinary skill in the art at the time of the invention to use a serial link with a

pair of simplex links for sending information in opposite directions as shown by Hong in the system of Conway in order to facilitate the fast transmission of data between the interfaces.

As for claim 49, the argument for claim 48 applies. Hong also shows that the simplex links are driven for differential signal transfers (col.3,lines 28-32).

Response to Arguments

11. Applicant should submit an argument under the heading "Remarks" pointing out disagreements with the examiner's contentions. Applicant must also discuss the references applied against the claims, explaining how the claims avoid the references or distinguish from them.

Applicant has not provided any remarks or arguments regarding the previous rejection. In a telephone conversation with applicant's representative in order to determine the status of the application, Mr. Klinger indicated that a response had been filed to the previous action but that response was not received in this case. The amendment filed 25 April 2005 does not include any arguments.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited references are all referred to in the specification but do not appear to have been cited on either the previous PTO-892 or in an IDS.

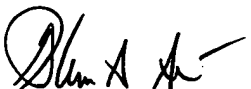
13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn A. Auve whose telephone number is (571) 272-3623. The examiner can normally be reached on M-F 8:00 AM-5:30 PM, every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (571) 272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Glenn A. Auve
Primary Examiner
Art Unit 2111

gaa
6 July 2005